Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously presented) A method comprising:

causing to receive in a queue manager a first enqueue or dequeue request with respect to a queue;

causing to receive in the queue manager a second enqueue or dequeue request with respect to the queue;

causing to commence processing of the second request prior to completion of processing the first request; and

causing to store information describing a structure of the queue in a cache memory implemented in a distributed manner.

2. (Original) The method of claim 1 including causing to modify stored information describing a structure of the queue in response to the requests.

3. (Previously presented) The method of claim 2 including causing to store the modified information in the cache memory.

4. (Previously presented) The method of claim 1 including causing to store data in the queue related to the first and second requests using a linked list data structure.

5. (Original) The method of claim 1 wherein the first request is an enqueue request and the second request is a dequeue request.

6. (Original) The method of claim 1 wherein the first request is a dequeue request and the second request is an enqueue request.

7. (Original) The method of claim 1 wherein the first request is an enqueue request and the second request is an enqueue request.

8. (Original) The method of claim 1 wherein the first request is a dequeue request and the second request is a dequeue request.

9. (Previously presented) An apparatus comprising:

a processing engine to make enqueue requests;

a scheduler to make dequeue requests;

a cache memory to store data describing a structure of a queue;

a memory controller to initiate queue commands; and

a queue manager including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to the same queue is being processed,

wherein the cache memory is distributed partially to the memory controller.

10. (Previously presented) The apparatus of claim 9 further including memory to store data placed on a queue wherein the memory includes a linked list data structure.

11. (Original) The apparatus of claim 9 wherein the processing engine includes a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

12. (Original) The apparatus of claim 9 including a second plurality of multi-threaded pipelined programming engines, configured as a second pipeline to receive data from the queue manager and send data to a transmit buffer.

13. (Original) The apparatus of claim 9 wherein the scheduler includes multi-threaded pipelined programming engines, the scheduler configured to determine the order of packets to be removed from the queue and to store a bit for the queue indicating whether the queue is empty.

14. (Original) The apparatus of claim 9 wherein the queue manager is configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the cache memory is coherent with entries in the content addressable memory.

15. (Previously presented) A system comprising:

a source of data packets;

a destination of data packets; and

a device operating to transfer data packets from the source to the destination comprising:

a processing engine to make enqueue requests;

a scheduler to make dequeue requests;

a cache memory to store data describing a structure of a queue;

a memory controller to initiate queue commands; and

a queue manager including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, the queue manager configured to process the enqueue requests and the dequeue requests and capable of processing a request to a queue while a previous request with respect to the same queue is being processed;

wherein the apparatus is connected to a high line rate, and

further wherein the cache memory is distributed partially to the memory controller.

16. (Previously presented) The system of claim 15 further including a memory to store data placed on a queue wherein the memory includes a linked list data structure.

17. (Original) The system of claim 15 wherein the processing engine includes a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

18. (Original) The system of claim 15 further including a second plurality of multi-threaded pipelined programming engines, configured as a second processing engine to receive data from the queue manager and send data to a transmit buffer.

19. (Original) The system of claim 15 wherein the scheduler includes multi-threaded pipelined programming engines, the scheduler configured to determine the order of packets to be removed from the queue and store a bit for each queue indicating whether the queue is empty.

20. (Original) The system of claim 15 wherein the queue manager is configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the memory controller is coherent with the entries in the content addressable memory.

21. (Previously presented) An article comprising a computer-readable medium including computer-readable instructions that, when applied to a computer system, cause the computer system to:

commence processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with respect to the same queue and

store information that describes a structure of the queue in a distributed cache memory.

22. (Original) The article of claim 21 including instructions that cause the computer system to:

modify stored information describing a structure of the queue in response to the requests.

23. (Previously presented) The article of claim 22 including instructions that cause the computer system to:

store the modified information in the cache memory.

24. (Previously presented) The article of claim 21 including instructions that cause the computer system to:

store data in the queue related to the first and second requests using linked list data structures.

25. (Original) The article of claim 21 including instructions that cause the computer system, in response to receiving an enqueue request with respect to the queue and a subsequent dequeue request with respect to the queue, to:

commence processing of the dequeue request prior to completion of processing the enqueue request.

26. (Original) The article of claim 21 including instructions that cause the computer system in response to receiving a dequeue request with respect to the queue and a subsequent enqueue request with respect to the queue, to:

commence processing of the enqueue request prior to completion of processing the dequeue request.

27. (Original) The article of claim 21 including instructions that cause the computer system, in response to receiving a first enqueue request with respect to the queue and a subsequent second enqueue request with respect to the queue, to:

commence processing of the second request prior to completion of processing the first request.

28. (Original) The article of claim 21 including instructions that cause the computer system, in response to receiving a first dequeue request with respect to the queue and a subsequent second dequeue request with respect to the queue, to:

commence processing of the second request prior to completion of processing the first request.

29. (Previously presented) The method of claim 1 wherein the cache memory are distributed to the queue manager and a memory controller.

30. (Previously presented) The method of claim 1 wherein the cache memory are distributed to a memory controller and a memory residing externally to a network processor.

31. (Previously presented) The apparatus of claim 9 wherein the cache memory are distributed partially to the queue manager.

32. (Previously presented) The apparatus of claim 9 further including a memory adapted to store a queue of buffers wherein the cache memory are distributed partially to the memory adapted to store the queue of buffers.

33. (Previously presented) The system of claim 15 wherein the cache memory are distributed partially to the queue manager.

34. (Previously presented) The system of claim 15 further including a memory adapted to store a queue of buffers wherein the cache memory are distributed partially to the memory adapted to store a queue of buffers.

35. (New) The method of claim 1 comprising:

issuing commands to return data describing the structure of the queue and

fetching data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue is coherent with entries in a content addressable memory.